IN THE CLAIMS:

1. (Currently Amended): A method for measuring shared contact resistance in a memory cell design, the method comprising:

providing a first test array of main test structures based on a real memory product, wherein each main test structure includes at least one shared contact and wherein the first test array builds a chain of shared contact resistance from a first contact point to a second contact point;

applying voltage to the first test array from the first contact point to the second contact point; [[and]]

measuring shared contact resistance in the chain of shared contact resistance;

providing a second test array of first supplemental test structures based on the real memory product, wherein each first supplemental test structure includes at least one shared contact and wherein the second test array builds a chain of shared contact resistance on a silicon island side of the shared contacts in the second test array from a first contact point to a second contact point;

applying voltage to the second test array from the first contact point to the second contact point; and

measuring silicon island side resistance in the chain of shared contact resistance on the silicon island side of the shared contacts in the second test array.

2. (Canceled)

3. (Currently Amended): The method of claim [[2]] 1, further comprising:

subtracting the measured silicon island side resistance from the measured shared contact resistance to determine a poly side resistance.

4. (Original): The method of claim 1, further comprising:

providing a third test array of second supplemental test structures based on the real memory product, wherein each second supplemental test structure includes at least one shared contact and wherein the third test array builds a chain of shared contact

resistance on a poly side of the shared contacts in the third test array from a first contact point to a second contact point;

applying voltage to the third test array from the first contact point to the second contact point; and

measuring poly side resistance in the chain of shared contact resistance on the poly side of the shared contacts in the third test array.

5. (Original): The method of claim 4, further comprising:

subtracting the measured poly side resistance from the measured shared contact resistance to determine a silicon island side resistance.

6. (Original): The method of claim 1, further comprising:

providing a fourth test array of third supplemental test structures based on the real memory product, wherein the fourth test array builds a chain of silicon island connection line resistance in the fourth test array from a first contact point to a second contact point;

applying voltage to the fourth test array from the first contact point to the second contact point; and

measuring silicon island connection line resistance in the chain of silicon island connection line resistance in the fourth test array.

7. (Original): The method of claim 6, further comprising:

subtracting the measured silicon island connection line resistance from the measured shared contact resistance.

8. (Original): The method of claim 6, further comprising:

providing a fifth test array of fourth supplemental test structures based on the real memory product, wherein the fifth test array builds a chain of poly connection line resistance in the fifth test array from a first contact point to a second contact point;

applying voltage to the fifth test array from the first contact point to the second contact point; and

measuring poly connection line resistance in the chain of poly connection line resistance in the fifth test array.

9. (Original): The method of claim 8, further comprising:

subtracting the measured poly connection line resistance from the measured shared contact resistance.

10. (Original): The method of claim 8, further comprising:

subtracting the measured silicon island connection line resistance and the measured poly connection line resistance from the measured shared contact resistance.

11. (Currently Amended): An apparatus for measuring shared contact resistance in a memory cell design, the apparatus comprising:

a first test array of main test structures based on a real memory product, wherein each main test structure includes at least one shared contact and wherein the first test array builds a chain of shared contact resistance from a first contact point to a second contact point;

a tester, wherein the tester applies a voltage to the first test array from the first contact point to the second contact point and measures shared contact resistance in the chain of shared contact resistance;

a second test array of first supplemental test structures based on the real memory product, wherein each first supplemental test structure includes at least one shared contact and wherein the second test array builds a chain of shared contact resistance on a silicon island side of the shared contacts in the second test array from a first contact point to a second contact point,

wherein the tester applies a voltage to the second test array from the first contact point to the second contact point and measures silicon island side resistance in the chain of shared contact resistance on the silicon island side of the shared contacts in the second test array.

12. (Canceled)

13. (Currently Amended): The apparatus of claim [[12]] 11, wherein the tester subtracts the measured silicon island side resistance from the measured shared contact resistance to determine a poly side resistance.

14. (Original): The apparatus of claim 11, further comprising:

a third test array of second supplemental test structures based on the real memory product, wherein each second supplemental test structure includes at least one shared contact and wherein the third test array builds a chain of shared contact resistance on a poly side of the shared contacts in the third test array from a first contact point to a second contact point,

wherein the tester applies a voltage to the third test array from the first contact point to the second contact point and measures poly side resistance in the chain of shared contact resistance on the poly side of the shared contacts in the third test array.

15. (Original): The apparatus of claim 14, wherein the tester subtracts the measured poly side resistance from the measured shared contact resistance to determine a silicon island side resistance.

16. (Original): The apparatus of claim 11, further comprising:

a fourth test array of third supplemental test structures based on the real memory product, wherein the fourth test array builds a chain of silicon island connection line resistance in the fourth test array from a first contact point to a second contact point,

wherein the tester applies a voltage to the fourth test array from the first contact point to the second contact point and measures silicon island connection line resistance in the chain of silicon island connection line resistance in the fourth test array.

17. (Original): The apparatus of claim 16, wherein the tester subtracts the measured silicon island connection line resistance from the measured shared contact resistance.

18. (Original): The apparatus of claim 16, further comprising:

a fifth test array of fourth supplemental test structures based on the real memory product, wherein the fifth test array builds a chain of poly connection line resistance in the fifth test array from a first contact point to a second contact point,

wherein the tester applies voltage to the fifth test array from the first contact point to the second contact point and measures poly connection line resistance in the chain of poly connection line resistance in the fifth test array.

19. (Original): The apparatus of claim 18, wherein the tester subtracts the measured poly connection line resistance from the measured shared contact resistance.

20. (Original): The apparatus of claim 18, wherein the tester subtracts the measured silicon island connection line resistance and the measured poly connection line resistance from the measured shared contact resistance.